

TOWNSEND AND TOWNSEND AND CREW LLP
ERIC P. JACOBS (State Bar No. 88413)
PETER H. GOLDSMITH (State Bar No. 91294)
ROBERT A. McFARLANE (State Bar No. 172650)
IGOR SHOIKET (State Bar No. 190066)
Two Embarcadero Center, 8th Floor
San Francisco, California 94111
Telephone: (415) 576-0200
Facsimile: (415) 576-0300
E-mail: epjacobs@townsend.com
phgoldsmith@townsend.com
ramcfarlane@townsend.com
ishoiket@townsend.com

Attorneys for Defendant and Counterclaimant
FAIRCHILD SEMICONDUCTOR CORPORATION

UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

ALPHA & OMEGA SEMICONDUCTOR,
INC., a California corporation; and
ALPHA & OMEGA SEMICONDUCTOR,
LTD., a Bermuda corporation,
Plaintiffs and Counterdefendants,

v.

FAIRCHILD SEMICONDUCTOR
CORP., a Delaware corporation,
Defendant and Counterclaimant.

AND RELATED COUNTERCLAIMS.

Case No. C 07-2638 JSW
(Consolidated with Case No. C 07-2664 JSW)

**DECLARATION OF DR. RICHARD A.
BLANCHARD IN SUPPORT OF
FAIRCHILD SEMICONDUCTOR
CORPORATION'S REPLY TO AOS'S
OPPOSITION TO FAIRCHILD'S
MOTION TO COMPEL PRODUCTION
OF DOCUMENTS**

Date: September 16, 2008
Time: 2:00 p.m.
Courtroom: E, 15th Floor
Hon. Elizabeth D. Laporte

REDACTED PUBLIC VERSION

1 I, Dr. Richard A. Blanchard, declare as follows:

2 1. I have been retained as an expert regarding semiconductor technology by Defendant
3 and Counterclaimant Fairchild Semiconductor Corporation ("Fairchild"). This declaration is
4 submitted in support of Fairchild's Reply in support of its Motion to Compel Production of
5 Documents ("Motion to Compel"). I provided information concerning my background and experience
6 in my declaration dated August 12, 2008 in support of the Motion to Compel (the "August 12
7 Declaration"), which I am incorporating by reference into this declaration. I have personal knowledge
8 of the matters stated herein and if called to testify as a witness, I could and would competently testify
9 thereto.

10 2. AOS's process flows describe at a *general level* the manufacturing steps used for
11 making AOS's products. They provide a sequence of steps used to make the device. The process
12 flows, however, do not provide all of the *details* concerning each step in the manufacturing process.
13 Such details, which can be used as input data for simulation software used to model the structure and
14 operation of a device, are typically found in recipes.

15 3. As I explained in my August 12 Declaration, the Fairchild Mo Patents claim a novel
16 way of controlling the phenomenon of breakdown in the active area of power MOSFETs.¹ U.S. Patent
17 No. 6,818,947 ("the '947 patent") claims a novel way of forming structures that increase breakdown
18 voltage in the termination region of a power semiconductor device. Breakdown is an unwanted effect
19 where current flows between the source and drain terminals even if no voltage is applied to the gate,
20 i.e., the device is conducting ("on") when it should not be conducting ("off"). Generally, current can
21 flow easily in only one direction across a P-N junction formed in a semiconductor device. This occurs
22 when the P-N junction has voltage applied across it in the forward direction. If, however, the polarity
23 of the voltage is reversed across the junction, current will not flow unless the voltage is increased to
24 the point that current carriers gain enough energy to knock other current carriers free from the silicon

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26 ¹ In this declaration, the term "Fairchild Mo Patents" refers to U.S. Patent Nos. 6,429,481 ("the '481
27 patent"), 6,521,497 ("the '497 patent"), 6,710,406 ("the '406 patent"), 6,828,195 ("the '195 patent"),
28 and 7,148,111 ("the '111 patent").

1 lattice. This generally unwanted effect is named "avalanche breakdown." The reverse voltage at
2 which a power MOSFET will experience avalanche breakdown is referred to as its "breakdown
3 voltage."

4 4. Power MOSFET designers go to great lengths to control breakdown because it can
5 irreversibly damage the device. The Fairchild Mo Patents address the important goal of avoiding
6 having the device go into breakdown near the fragile gate structure formed in the trenches. If
7 breakdown occurs near the gate, the thin gate oxide surrounding the gate electrode in the trench can be
8 damaged. The Fairchild Mo Patents claim a novel method and design for forming a heavy body
9 region in the well which serves to insure that breakdown current is spaced away from the trenches. If
10 the breakdown current is spaced away from the trenches, the device will have a much better chance of
11 surviving the breakdown event, a characteristic that is referred to as "ruggedness." By enhancing
12 power MOSFET ruggedness, the Fairchild Mo Patents achieve an important goal of power MOSFET
13 design. The '947 patent, on the other hand, combines previously separate structures in the termination
14 region into a contiguous structure. This combined structure provides for increased breakdown voltage
15 in the termination region while advantageously reducing the amount of surface area that must be
16 devoted to termination structures, allowing for a larger active region.

17 5. As I explained in my August 12 Declaration, the claims of the Fairchild Mo Patents
18 relate to the manufacture, structure, and operation of power MOSFET devices. Structural features to
19 which the claims relate include the presence or absence of an "abrupt junction." *See, e.g.,* '481 patent,
20 claim 1. Operational features to which the claims relate include the location of the breakdown
21 initiation point, the location of the peak electric field, and the uniformity of the avalanche current in
22 the device. *See, e.g.,* '481 patent, claim 1 ("so that a transistor breakdown initiation point is spaced
23 away from the trench"); '111 patent, claim 29 ("so that peak electric field is moved away from a
24 nearby trench toward the heavy body"); '111 patent, claim 29 ("resulting in avalanche current that is
25 substantially uniformly distributed").

26 6. The claims of the '947 patent relate to the manufacture, structure, and operation of
27 power semiconductor devices. Structural features to which the claims of the '947 relate include gate
28 runners, contacts, feeds, and isolation trenches located within the termination region of the device, as

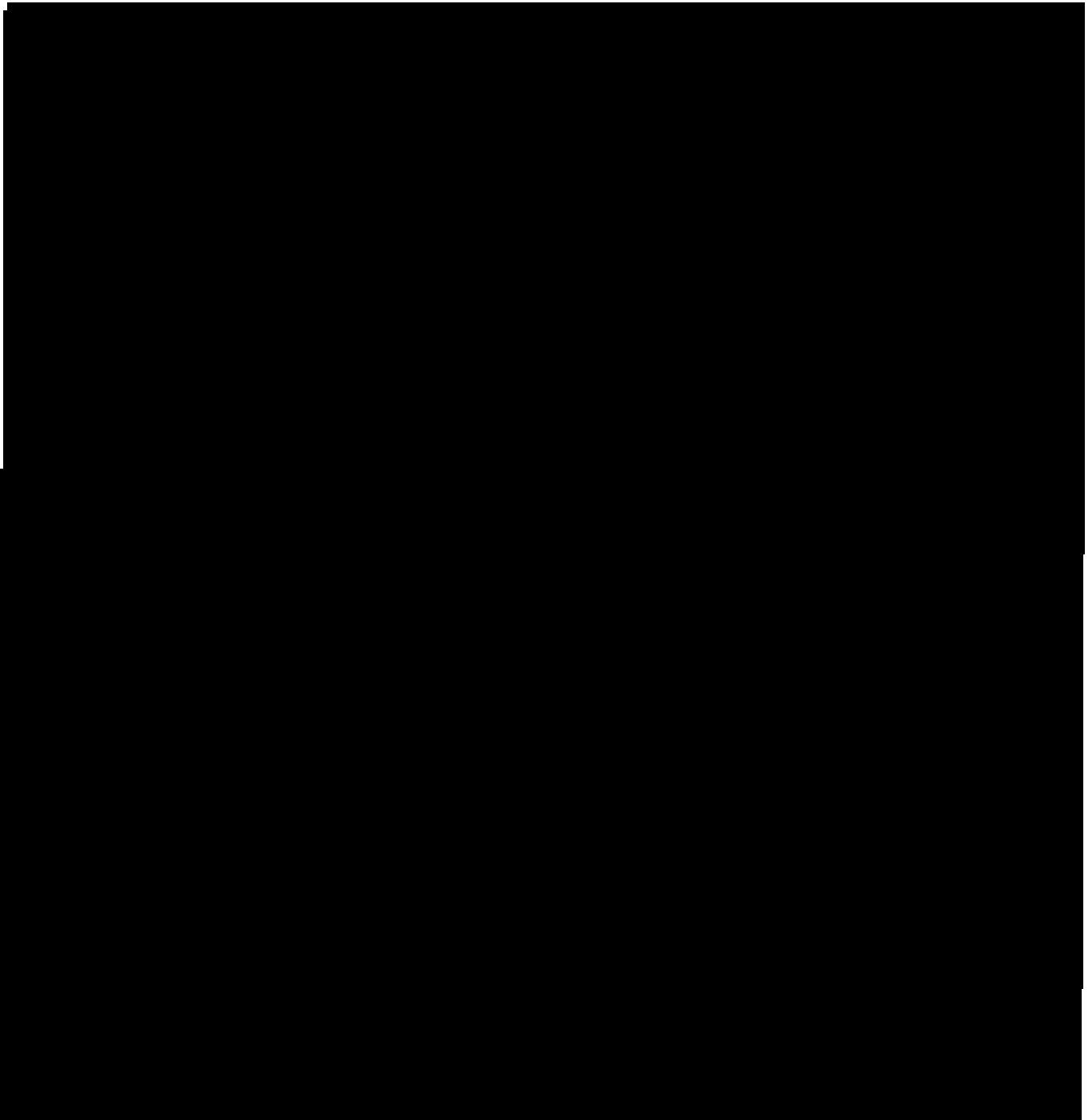
1 well as trenched gate runners extending across the active region of the device. *See, e.g.*, '947 patent,
2 claim 1 (“including a contact ...,” “including a feed ...,” “an isolation trench ...”); claim 5 (“forming
3 a trenched gate runner”); and claim 6 (“a plurality of elongated inner runners”). Operational features
4 to which the claims relate include increasing breakdown voltage in the termination region. *See, e.g.*,
5 '947 patent, claim 1 (“acting as a field plate to extend the device breakdown voltage in the termination
6 region ...”).

7 7. The operational features of power MOSFET devices, including the features described
8 above, can be affected by a variety of factors, including the shape, location and dopant profile of
9 regions in the device, the shape and depth of the trenched gate and trenched gate runner and the
10 thickness of the gate oxide. Information regarding these factors, in turn, may be deciphered from
11 information concerning how the device was made, which often is included in the recipes used in
12 manufacturing the trench, doped well, heavy body, and other regions of the device. Once this
13 information is gleaned from the recipes and other sources, simulation software can be used to
14 determine the structure and operational features of a device.

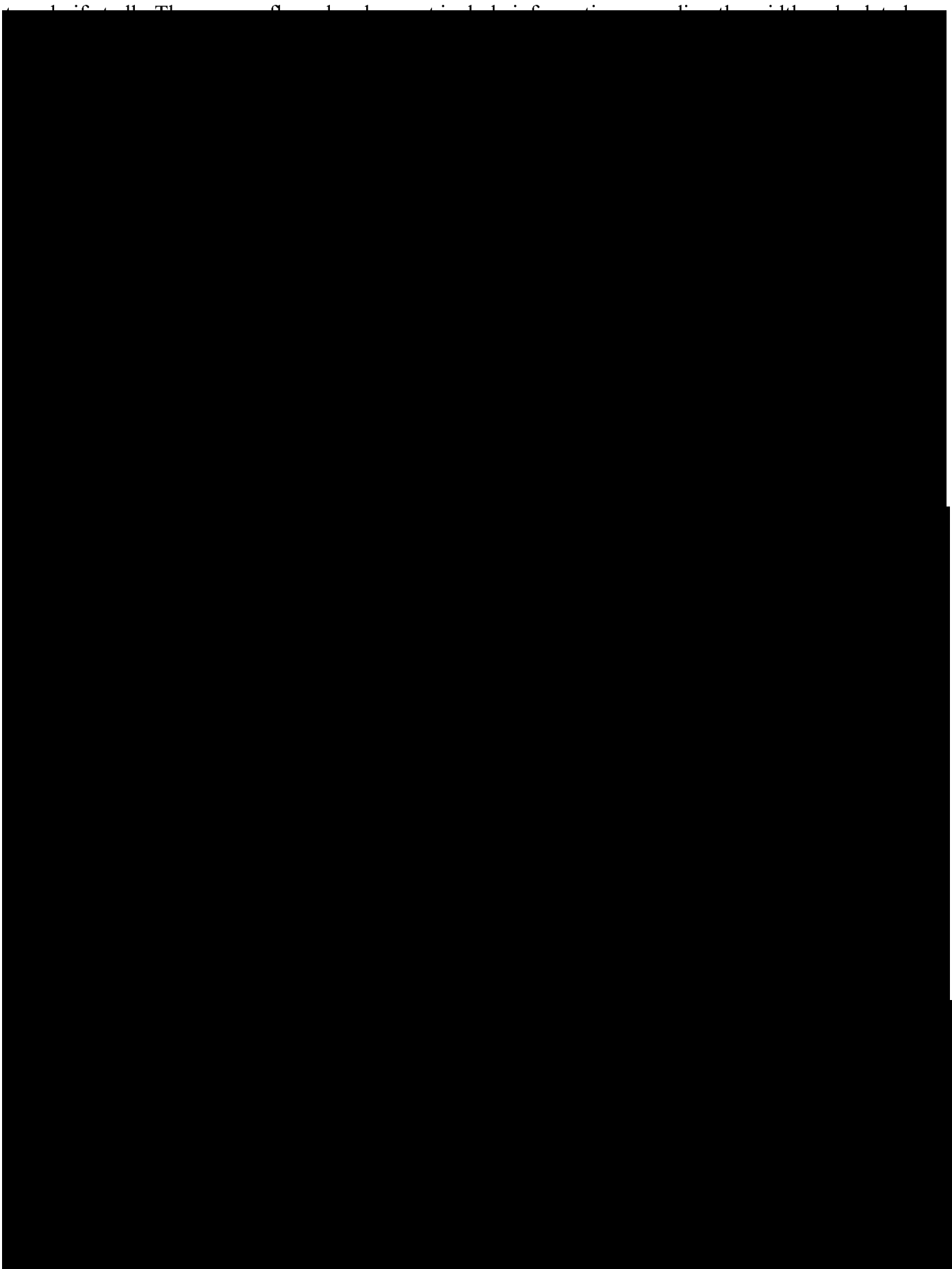
15 8. Power MOSFET device designers routinely conduct computer simulations to analyze
16 device operational characteristics, including features such as the locations of breakdown initiation and
17 peak electric field, the characteristics of the avalanche current and the characteristics of breakdown
18 voltage. They typically use recipe information when simulating these characteristics in combination
19 with other information. Simulation programs, for example, typically require input information such as
20 oxidation recipes, implant recipes, implant drive recipes, polysilicon deposition recipes, polysilicon
21 doping recipes, etch recipes, and critical dimension measurement recipes for well, source, contact, and
22 trench regions of the device. The simulation programs use such information to analyze the structure
23 and operation of the device, including operational features such as the location of the breakdown
24 initiation point and peak electric field and the characteristics of the avalanche current for the Fairchild
25 Mo Patents, and the characteristics of the breakdown voltage for the '947 patent. Because the
26 accuracy of results obtained from simulation software generally increases with more complete and
27 accurate input data, information that might not immediately appear relevant to particular structural or
28 operational features may in fact be helpful in performing a device simulation of such structural or

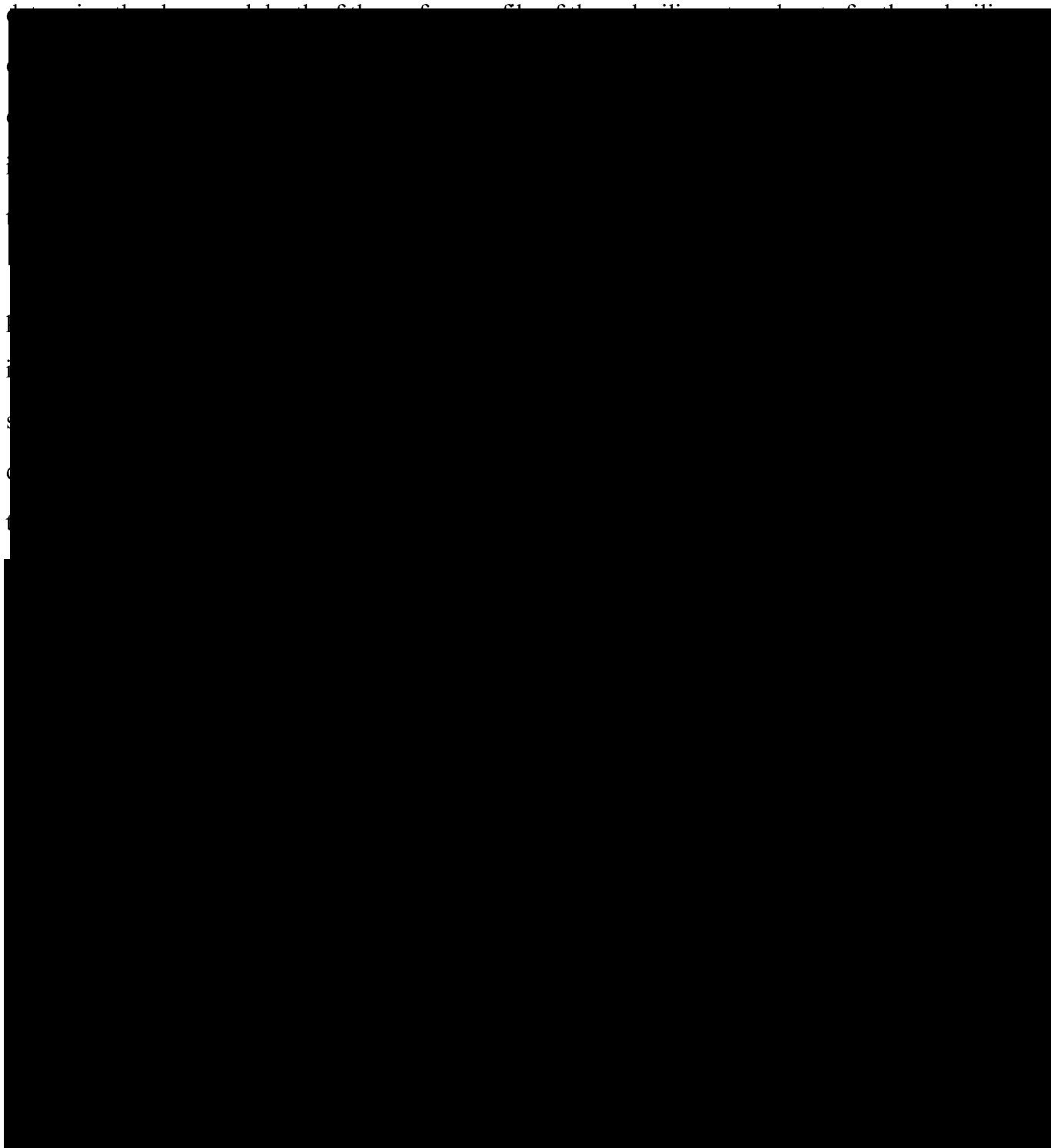
1 operational features.

2 9. Process flows describe at a high level the sequence of steps in the manufacturing
3 process, including the order of deposition, etch, implant and diffusion steps. Process flows typically
4 include a name or very brief description of each step, but do not contain all of the details concerning
5 that step. For this reason, process flows typically do not provide all the information helpful in
6 performing accurate and complete simulations. Such information is typically found in the recipe
7 associated with that step.



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17. As I explained in my August 12 Declaration, in the semiconductor field, "in-line data"

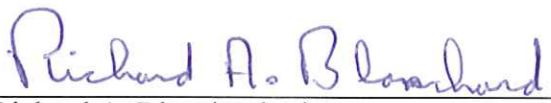
² Isotropic means etching uniformly in all directions, while anisotropic means etching primarily in one direction.

1 is collected from devices during the manufacturing process. This data typically includes information
2 concerning the structural features of the devices, such as the location and dimensions of various
3 structural features, including the depths of trenches, doped wells, and other features relevant to many
4 asserted claim elements of the Fairchild Mo patents, and the gate runners, contacts and other structural
5 features relevant to asserted claim elements of the '947 patent. Additionally, in-line data can be used
6 as input information for simulations of AOS's accused products.

7 18. Although in-line data is collected from individual wafers, it is typically collected over
8 the duration of manufacturing for each part and collated into *average measurements* and *standard*
9 *deviations* over a period of time. These average measurements and standard deviations reflect the
10 "real world" structural measurements of devices manufactured and sold over that time period. This
11 data is typically reviewed and analyzed periodically to verify that the manufacturing processes and
12 tools are meeting device specifications. In my experience, the in-line data is typically collected and
13 stored in a way to facilitate this review and analysis, generally in a single database.

14
15 I declare under penalty of perjury under the laws of the United States of America that the
16 foregoing is true and correct to the best of my knowledge and belief.

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18 Executed this 3rd day of September, 2008, in Mountain View, California.

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21 Richard A. Blanchard, Ph. D.

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